WHAT IS CLAIMED IS:

1. A method of fixing a faulty line or lines of operating code for delivery to a processor from a ROM contained in a location of said ROM designated by an address, said operating code being requested by said processor, comprising the steps of:

providing a RAM having address locations, operating code locations associated with said address locations, and at least two flag bit locations associated with at least one of said address location;

identifying said line or lines of said faulty operating code in said ROM;

writing and storing correct line or lines of code in said RAM at said address location in RAM for each location of said faulty code in ROM starting at the first line of faulty code sequence and storing the address of said first line of faulty code in said RAM,

setting a start flag at one flag bit location at said address of said correct code in said RAM;

setting an end flag at said second flag bit location on the last line of correct code in said RAM;

snooping said RAM for an address indicated by said start flag and, when found, delivering said correct code to said processor in place of said faulty code from said ROM until a line of code has an end bit flag; and

returning to said ROM after said replacement code at said location of said detected end bit has been delivered.

2. The invention as defined in claim 1 wherein a continue flag is set in each line of replacement code when a line of replacement code follows that line.

3. The invention as defined in claim 1 wherein the number of lines of said replacement code is different from the number of lines of said faulty operating code being replaced by said lines of replacement code, and said final line of said replacement code is a jump instruction back to said operating code.

4. The invention as defined in claim 3 wherein there are fewer lines of said replacement code than lines of said faulty operating code being replaced.

5. The invention as defined in claim 3 wherein there are more lines of replacement code than lines of said faulty operating code being replaced.

6. The invention as defined in claim 1 wherein there is a flush cache instruction delivered to said processor after said last line of replacement code has been acted on.

7. The invention as defined in claim 2 wherein an error message is returned if neither a continue flag nor an end flag is set at an address of said replacement code.

8. The invention as defined in claim 1 wherein a multiplexer is provided to selectively deliver either said original operating code or said replacement code.

9. The invention as defined in claim 1 wherein a control device is provided to deliver either said original operating code or said replacement code to said processor.

10. The invention as defined in claim 8 wherein a control device operates said multiplexer.

11. An integrated circuit (I/C) chip having thereon a program for fixing a faulty line or lines of operating code for delivery to a processor from a ROM on said I/C chip, said operating code contained in a location on said ROM designated by an address, said operating code being requested by said processor, and a RAM on said I/C chip having address locations, operating code locations associated with said address locations and at least two flag bit locations associated with at least one of said address locations; said program comprising;

identifying said line or lines of said faulty operating code in said ROM;

writing and storing correct line or lines of code in said RAM at said address location in RAM for each location of said faulty code in ROM starting at the first line of faulty code sequence and storing said address of said first line of faulty code in said RAM,

setting a start flag at one flag bit location at said address of said correct code in said RAM;

setting an end flag at said second flag bit location on the last line of correct code in said RAM;

snooping said RAM for an address indicated by said start flag and, when found, delivering said correct code to said processor in place of said faulty code from said ROM until a line of code has an end bit flag; and

returning to said ROM after said replacement code at said location of said detected end bit has been delivered.

12. The invention as defined in claim 11 wherein a continue flag is set in each line of replacement code when a line of replacement code follows that line.

13. The invention as defined in claim 11 wherein the number of lines of said replacement code is different from the number of lines of said faulty operating code being replaced by said lines of replacement code, and the final line of said replacement code is a jump instruction back to said operating code.

14. The invention as defined in claim 13 wherein there are fewer lines of replacement code than line of said faulty operating code being replaced.

15. The invention as defined in claim 13 wherein there are more lines of replacement code than line of said faulty operating code being replaced.

16. The invention as defined in claim 11 wherein there is a flush cache instruction delivered to said processor after said last line of replacement code has been acted on.

17. The invention as defined in claim 12 wherein an error message is returned if neither a continue flag nor an end flag is set at an address of said replacement code.

18. The invention as defined in claim 11 wherein a multiplexer is provided to selectively deliver either said original operating code or said replacement code.

19. The invention as defined in claim 11 wherein a control device is provided to deliver either said original operating code or said replacement code to said processor.

20. The invention as defined in claim 18 wherein a control device operatives said multiplexer.